REMARKS

Reconsideration of the above identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1-9 are pending in this application.

In the Office Action, Claims 1, 2, 7 and 8 were rejected under 35 U.S.C. §102(a) over the applicant's admitted prior art (AAPA). The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

The Examiner notes on page 2, lines 9-12 of the Office Action that "...electrode portions 118 of an N+ buried layer 102 formed to isolate the P-type silicon substrate and the plurality of vertical pnp transistors from each other are provided in an active region of the power transistor". This assertion is incorrect for the following reasons. First, the N+ type electrode layer 118 of N+ buried layer 102 of AAPA is not provided in a power transistor active region, which is between a P+ type collector layer 106 and a P+ type collector layer 106. Referring to Figure 4 in particular, the active region is illustrated under the indicated bracket and **118 is outside this bracket**. Second, if an N+ type electrode layer 118 of N+ type buried layer 102 of AAPA **were** provided in a power transistor active region, the N+ type electrode layer 118 of N+ type buried layer 102 **must** pass through the P+ type collector buried layer 103 of a vertical PNP transistor to be connected to the N+ type buried layer 102. However, the prior art of Figures 4 and 5 do **not** show N+ type electrode layer 118 passing through the P+ type collector buried layer 103. Accordingly, the N+ type electrode layer 118 of AAPA is not provided in a power transistor active region. Additionally, the N+ type electrode layer 118 of AAPA is formed so as to surround the P+ type collector layer 106, as described at page 2, lines 14-

17 of the subject application. Thus, it is apparent that the N+ type electrode layer 118 of AAPA is outside of an active region of the power transistor.

In contrast, Claim 1 recites a power transistor composed of a plurality of vertical PNP transistors formed on a P-type silicon substrate, wherein a singularity or plurality of electrode portions of an N^+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other are provided in an active region of the power transistor. The AAPA does not disclose or suggest such a structural configuration. Accordingly, Claim 1 and each of the claims depending therefrom distinguish the subject invention from the AAPA and withdrawal of the rejection is respectfully requested.

In the Office Action, Claims 1-8 were rejected under 35 U.S.C. § 103 (a) over the AAPA in view of U.S. Patent No. 5,648,281 to Williams et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

As noted above, the AAPA merely discloses a N^+ type electrode layer 118 outside the active region of a power transistor.

Williams et al. do not add anything relevant to the AAPA. Williams et al. disclose P+ sinkers 346 surrounding a PNP transistor 330 (see col. 24, line 23) and an N+ sinker 348 surrounding a P-well 344 (see col. 24, line 35). The active region of the PNP transistor in Williams et al. is inside of the P+ sinkers 346. Neither Figure 28 nor Figure 28A of Williams et al. disclose an electrode portion between the P+ sinkers 346 and which passes through a P buried layer 342 to an N buried layer 340. Thus, there is no teaching, motivation or suggestion in Williams et al. to provide an electrode portion of the N+ buried layer 340 in the power transistor active region.

In view of the above limitation with respect to Williams et al., it is apparent that Williams et al. do not overcome the deficiencies of the AAPA, as noted above with respect to Claim 1 and in the specification itself. In particular, neither the AAPA nor Williams et al. disclose or suggest, either alone or in combination, in whole or in part, a power transistor including, *inter alia*, a singularity or plurality of electrode portions of an N^+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other are provided in an active region of the power transistor. Accordingly, Claim 1 and each of the claims depending therefrom are not rendered obvious by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

In the Office Action, Claim 9 was rejected under 35 U.S.C. § 103 (a) over the AAPA in view of U.S. Patent No. 5,648,281 to Williams et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

As noted above, neither the AAPA nor Williams et al. disclose electrode portions of a N+ buried layer in an active region of a power transistor. Thus, there is nothing in either of these references that discloses or suggests, either alone or in combination, in whole or in part, the device defined by Claim 9 of the subject application. In particular, there is nothing in either the AAPA or Williams et al. which discloses or suggests, alone or in part, in whole or in combination, a power transmitter that includes a plurality of vertical PNP transistors formed on a P-type substrate, each PNP transistor having a P^+ type collector, an N+ type base well formed at a base region, a P^+ type emitter layer and an N^+ type base layer, an N^+ type buried layer isolating the P-type substrate from the P^+ type collector, an N-type epitaxial layer formed over a surface of the P-type

substrate, an N^+ type electrode layer and a plurality of N^+ type diffusion layers formed at electrode portions within an active region just under the N^+ type electrode layer to reduce resistance of the N-type epitaxial layer by extending therethrough to the N^+ type buried layer. Thus, for at least this reason, Claim 9 is not obvious in view of the cited combination and allowance is respectfully requested.

It is respectfully submitted that all of the claims now remaining in this application, namely Claims 1-9, are in condition for allowance, and such action is earnestly solicited. Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

Respectfully submitted,

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